What is claimed is:

1   Claim 1. In a software driven emulator comprised of a
2 plurality of modules on printed circuit boards, each of said
3 modules including a processor chip and at least one SDRAM
4 coupled to the processor chip, a maintenance bus coupled to
5 said SDRAM, and a memory controller coupled to said
6 maintenance bus, a method executing bulk data transfers to
7 said SDRAM via said maintenance bus, including the steps of:
8   transferring data to said SDRAM via said
9 maintenance bus on each clock cycle for a predetermined
10 number of clock cycles in succession;
11   halting the transfer of data after said
12 predetermined number of data transfers;
13   initiating a SDRAM refresh cycle after said
14 halting step;
15   resuming said transferring step upon receipt
16 of a done signal after said refresh cycle.

1   Claim 2. In a software driven emulator comprised of a
2 plurality of modules on printed circuit boards, each of said
3 modules including a processor chip and at least one SDRAM
4 coupled to the processor chip, a maintenance bus coupled to
5 said SDRAM, and a memory controller coupled to said
6 maintenance bus, a method executing bulk data transfers to
7 said SDRAM via said maintenance bus, including the steps of:
8   transferring data from said SDRAM via said
9 maintenance bus on each clock cycle for a predetermined
10 number of clock cycles in succession;
11   halting the transfer of data after said
12 predetermined number of data transfers;
13   initiating a SDRAM refresh cycle after said
14 halting step;

15   resuming said transferring step upon receipt

16 of a done signal after said refresh cycle.

1   Claim 3.   A method of executing bulk transfers as in claim 1

2   including establishing a starting address for said bulk

3   transfer in said memory controller and incrementing said

4   starting address by one on each clock cycle.

1   Claim 4.   A method of executing bulk transfers as in claim 2

2   including establishing a starting address for said bulk

3   transfer in said memory controller and incrementing said

4   starting address by one on each clock cycle.

1   Claim 5.   A method of executing bulk transfers as in claim 1

2   wherein a data word is transferred on each clock cycle.

1   Claim 6.   A method of executing bulk transfers as in claim 2

2   wherein a data word is transferred on each clock cycle.

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